

Appl. No. : **10/840,198**
Filed : **May 5, 2004**

REMARKS

The June 21, 2005 Office Action was based upon pending Claims 1-9 and 30-40. This Amendment amends Claims 1, 4, and 7. Thus, after entry of this Amendment, Claims 1-9, and 30-40 are pending and presented for further consideration.

In the June 21, 2005 Office Action, the Examiner rejected Claims 1-9 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,888,734 in view of U.S. Patent No. 6,349,051.

In addition, the Examiner rejected Claims 1-9 and 30-40 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,011,710 ("the Wiggers patent") in view of U.S. Patent No. 5,815,462 ("the Konishi patent").

DOUBLE PATENTING REJECTION OF CLAIMS 1-9

The Examiner rejected Claims 1-9 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,888,734 in view of U.S. Patent No. 6,349,051.

In response, Applicant submits herewith a Terminal Disclaimer in compliance with 37 C.F.R. §1.321(b) and (c). Applicant respectfully requests that the obviousness-type double patenting rejection be withdrawn.

REJECTION OF CLAIMS 1-9 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-9 and 30-40 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,011,710 ("the Wiggers patent") in view of U.S. Patent No. 5,815,462 ("the Konishi patent").

Claims 1, 4, and 7

Wiggers appears to teach a switch between a memory device and a data bus on a printed circuit board. Wiggers also appears to teach a memory controller controlling the switch. Wiggers does not teach a state decoder controlling the switch.

Konishi appears to teach a state decoder controlling a transfer gate in a data latency register configured as an inverter latch. The outputs of the inverter latch appear

to be used as control signals for switching a clock signal in a synchronous memory device.

Konishi does not teach a switch configured to decouple a data bus from a memory circuit when no memory access is being requested by the memory controller to reduce the parasitic capacitance of the data bus. Thus, there is no suggestion or motivation to combine the Konishi reference with the Wiggers reference used for reducing the parasitic capacitance of a data bus when no memory accesses are being requested by the memory controller.

In contrast, in an embodiment of the invention, a state decoder controls the switch, where the switch is configured to decouple a data bus from a memory circuit; when no memory access is being requested by the memory controller to reduce the parasitic capacitance of the data bus.

Because the references cited by the Examiner do not disclose, teach, or suggest the use of a state decoder interfacing with the memory controller and the switch such that the state decoder controls the switch to decouple the data bus from the memory circuit when no memory access is being requested by the memory controller to reduce the parasitic capacitance of the data bus, Applicant asserts that Claims 1, 4 and 7 are not obvious in view of Wiggers and Konishi. Applicant therefore respectfully submits that Claims 1, 4 and 7 are patentably distinguished over the cited references and Applicant respectfully requests allowance of Claims 1, 4, and 7.

Claims 2, 3, 5, 6, 8, 9, and 30-40

Claims 2, 3 and 30-33, which depend from Claim 1, Claims 5, 6 and 34-37, which depend from Claim 4, and Claims 8, 9, and 38-40, which depend from Claim 7, are believed to be patentable for the same reasons articulated above with respect to Claims 1, 4, and 7, respectively, and because of the additional features recited therein.

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CONCLUSION

Applicants have endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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